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(54) Title: METHOD AND SYSTEM FOR WAFER AND DEVICE-LEVEL TESTING OF AN INTEGRATED CIRCUIT

(57) Abstract: A tester comprises test logic and a connector for at least one device under test. The connector, which may comprise a wafer probe for dice on a wafer or a test fixture for packaged integrated circuit devices, has connections for the device under test that present an impedance selected to emulate the characteristic impedance of an end-use environment of the device under test. For example, in an embodiment in which the device under test comprises a logic device using Rambus Signaling Levels (RSL) to communicate to other devices and the end-use environment is connection to a Rambus channel, the characteristic impedance is between approximately 20 and 60 ohms. If, on the other hand, the end-use environment is connection to a Rambus memory module, then the characteristic impedance is approximately 28 ohms. Alternatively, if the end-use environment is connection to a DDR memory module, then the characteristic impedance is approximately 60 ohms. Thus, the tester of the present invention can accurately simulate operational behavior in an end-use environment of the device under test. Because this accurate simulation is available even for dice on a wafer, the needless expense associated with packaging defective dies and assembling defective dies into boards can be avoided. The test logic, which is coupled to the connector for communication with the deviceunder test, transfers test vectors and test data to the device under test. The test data and commands are utilized to perform multiples types of tests, including tests of the core logic and interface logic of the device under test. In this manner, the need for multiple types of testers is reduced or eliminated.

WO 01/63311 A2